AMENDMENT TO THE CLAIMS

Please amend the presently pending claims as follows:

1.(Currently Amended) Integrated circuit comprising means of delivering to at least one output a predetermined output voltage representative of a logic level, which comprises means of generating a main voltage and means of generating ~~an internal~~ a reference voltage lower than the main voltage, characterized in that it comprises

means of connecting the main voltage on the output, and

means of limiting and/or detecting the voltage on the output at the value of the predetermined output voltage, equal to the ~~internal~~ reference voltage, ~~taking into account the reference voltage,~~ and which comprises at least a second transistor having a gate connected to the gate of a third transistor mounted as a diode at the reference voltage.

2.(Cancelled)

3.(Currently Amended) Integrated circuit according to ~~claim 2~~ claim 1, characterized in that, when the predetermined voltage is reached, the currents circulating in the connecting means and in the limiting and/or detecting means are ~~balanced~~ comprised in the region of a few dozen µA.

4.(Currently Amended) Integrated circuit according to ~~claim 2~~ claim 1, characterized in that the connecting means comprise a first power transistor.

5.(Previously Presented) Integrated circuit according to claim 4, characterized in that the drain of the first power transistor is connected to the output and its source to the main voltage.

6. Canceled.

7. Canceled.

8.(Previously Presented) Integrated circuit according to claim 4, characterized in that the limiting means comprise means of blocking the first power transistor when the predetermined voltage is reached.

9.(Original) Integrated circuit according to claim 8, characterized in that the blocking means have first and second current mirrors connected to each other.

10.(Previously Presented) Integrated circuit according to claim 9, characterized in that the first current mirror delivers a blocking current when the predetermined voltage is reached on the output, and in that the second mirror sends a copy of the blocking current to the gate of the first power transistor, so as to block it.

11.(Previously Presented) Integrated circuit according to claim 4, characterized in that the gate of the first power transistor is connected to a command input via a fourth transistor.

12.(Currently Amended) Integrated circuit according to claim 10, characterized in that ~~the power of~~ the fourth transistor

is ~~less than that of~~ weaker than the transistors of the second mirror, so that the latter imposes its level on the fourth transistor when it delivers the copy of the blocking current.

13.(Original) Integrated circuit according to claim 1, characterized in that the output voltage corresponds to the logic level "1" of a USB connection.

14.(Original) Integrated circuit according to claim 1, characterized in that the reference voltage is used to supply the logic CMOS section of the integrated circuit.

15.(Previously Presented) Integrated circuit according to claim 1, characterized in that the reference voltage and/or the predetermined voltage have the value of 3 V, the main voltage having a value of 5 V.

16.(Currently Amended) Communication module for an integrated circuit comprising means of delivering, on at least one output, a predetermined output voltage representative of a logic level, which comprise means of generating a main voltage and means of generating ~~an internal~~ a reference voltage lower than the main voltage, characterized in that it comprises

means of connecting the main voltage to the output, and

means of limiting the voltage on the output at the predetermined output voltage value, ~~taking into account the reference voltage~~ which comprises at least a first transistor having a gate connected to the gate of a second transistor mounted as a diode at the reference voltage.

17-20.(Cancelled)

21.(Currently Amended) Integrated circuit comprising means of delivering to at least one output a predetermined output voltage representative of a logic level, which comprise means of generating a main voltage and means of generating ~~an internal~~ a reference voltage lower than the main voltage, characterized in that it comprises

means of connecting the main voltage on the output, which comprise a first power transistor, and

means of limiting and/or detecting the voltage on the output at the value of the predetermined output voltage, taking into account the reference voltage,

the limiting means comprising means of blocking the first power transistor when the predetermined voltage is reached,

the blocking means have first and second current mirrors connected to each other,

the first current mirror delivers a blocking current when the predetermined voltage is reached on the output, and in that the second mirror sends a copy of the blocking current to the gate of the first power transistor so as to block it,

the gate of the first power transistor being connected to a command input via a fourth transistor,

~~the power of~~ the fourth transistor is ~~less than that of~~ weaker than the transistors of the second mirror, so that the later imposes its level on the fourth transistor when it delivers the copy of the blocking current.

22. Canceled.

23. Canceled

24.(New) Integrated circuit comprising means of delivering to at least one output a predetermined output voltage representative of a logic level, which comprises means of generating a main voltage and means of generating a reference voltage lower than the main voltage, and comprising:

means of connecting the main voltage on the output and comprising a first power transistor, and

means of limiting and/or detecting the voltage on the output at the value of the predetermined output voltage, equal to the reference voltage, and comprising means of blocking the first power transistor when the predetermined voltage is reached, the means of blocking comprising first and second current mirrors connected to each other.

25.(New) Integrated circuit comprising means of delivering to at least one output a predetermined output voltage representative of a logic level, which comprises means of generating a main voltage and means of generating a reference voltage lower than the main voltage, and comprising:

means of connecting the main voltage on the output, and

means of limiting and/or detecting the voltage on the output at the value of the predetermined output voltage, equal to the reference voltage, and which comprises means of blocking the means of connecting when the predetermined voltage is reached, wherein the means of blocking comprises a first current mirror that delivers a

blocking current when the predetermined voltage is reached on the output and a second current mirror that sends a copy of the blocking current to the means of connecting, so as to block the means of connecting.

Thus, this Amendment is believed to clarify that, in the example described on page 10 of the present application, the currents circulating in the connecting means and in the limiting and/or detecting means are maintained in the region of a few dozen μA in order to maintain the USB capacity at 3V.

Claim 12 is amended to remove reference to the "power" of the fourth transistor and to clarify that "the fourth transistor is weaker than the transistors of the second mirror." Further, claim 12 is supported by the specification on page 11, lines 9-11, which states "the transistor TP5 [transistor of the second mirror TP4, TP5 in Figure 4] is configured in such a way that it is able to impose its level on transistor TN3 [fourth transistor, see page 6, line 3], the later [fourth transistor TN3] being a very weak transistor."

Claim 21 is amended in a similar fashion as claim 12.

With these amendments, Applicant respectfully requests that the rejection of claims 1, 3-15 and 21 under §112, second paragraph be withdrawn.

IV. CLAIM REJECTIONS UNDER §102 AND §103

Claims 1, 3-6 8, 11, 14, 16, 22 and 23 were rejected under §102(b) as being anticipated by Yamasaki, U.S. Patent No. 6,486,731. Claims 13 and 15 were rejected under §103(a) as being unpatentable over Yamasaki.

With this Amendment, independent claim 1 is amended to include the elements of dependent claims 6 and 7, which were indicated as being allowable if rewritten in independent form and to overcome the rejections under §112.

Similarly, independent claim 16 is amended to include the elements of dependent claims 6 and 7.

New claim 24 substantially corresponds to a combination of pending claims 1, 4, 8 and 9. New claim 25